Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Claim 1 (currently amended): Instruction Set Architecture (ISA) selection logic within a CPU for selecting an ISA decoding mode for a program instruction ~~from a plurality of ISA decoding modes, the program instruction retrieved from an address in an address space of the CPU~~, the selection logic comprising:

a plurality of boundary address registers for storing boundary addresses that partition ~~the~~ an address space into a plurality of address ranges, each of the plurality of address ranges corresponding to ~~the~~ one of a plurality of ISA decoding modes~~, wherein the size of an address range corresponds to the distribution of program instructions for the corresponding ISA decoding mode~~; and

an ISA mode controller ~~selection logic~~, coupled to ~~said~~ the plurality of boundary address registers, ~~for receiving the~~ that includes address evaluation logic,

wherein the ISA mode controller

receives an address of a program instruction to be decoded, ~~and for comparing~~

compares the address to ~~said~~ boundary addresses stored in the plurality of boundary address registers, and

determines ~~the~~ an ISA decoding mode for the program instruction based upon the comparison of the address to the boundary addresses.

Claims 2-8 (cancelled)

Claim 9 (currently amended): The selection logic ~~as recited in claim 8~~ of claim 1, wherein ~~said~~ the ISA mode controller ~~selection logic~~ provides the ISA decoding mode to an instruction decoder ~~decoding logic~~ to enable correct decoding of the program instruction.

Claims 10-17 (cancelled)

Claim 18 (currently amended): A ~~CPU for executing a~~ multiple-ISA mode processor ~~program~~, comprising:

an ISA mode controller that includes address evaluation logic ~~selection logic, configured to provide a first ISA mode indicator that corresponds to a first program instruction, said first program instruction being fetched from a first address in memory~~;

a plurality of ~~ISA mode~~ boundary address registers, coupled to ~~said~~ the ISA mode controller ~~selection logic, configured to store boundary addresses that partition said memory into address ranges, wherein a plurality of ISA modes is mapped to said address ranges, and wherein the size of an address range corresponds to the distribution of program instructions for the corresponding ISA mode~~; and

an instruction decoder, coupled to ~~said~~ the ISA mode controller, ~~selection logic, configured to receive said first ISA mode indicator, and configured to decode said first instruction according to said first ISA mode~~

wherein the ISA mode controller

receives an address of a program instruction to be decoded,

compares the address to boundary addresses stored in the plurality of boundary address registers,

determines an ISA decoding mode for the program instruction based upon the comparison of the address to the boundary addresses, and

provides the ISA decoding mode for the program instruction to the instruction decoder.

Claim 19 (cancelled)

Claim 20 (original): The ~~CPU~~ processor of ~~as recited in~~ claim 18, wherein boundary addresses stored in the plurality of boundary address registers partition an address space of the processor into a plurality of address ranges, each of the plurality of address ranges corresponding to one of a plurality of ISA decoding modes. ~~said ISA mode boundary address registers contain said boundary addresses that designate said address ranges.~~

Claims 21-35 (cancelled)

Claim 36 (new): The ISA selection logic of claim 1, wherein the plurality of boundary address registers store boundary addresses that represent lower address bounds for the plurality of address ranges.

Claim 37 (new): The ISA selection logic of claim 1, wherein the plurality of boundary address registers store boundary addresses that represent upper address bounds for the plurality of address ranges.

Claim 38 (new): The ISA selection logic of claim 1, wherein the plurality of boundary address registers store boundary addresses that partition the address space into a plurality of unequal address ranges.

Claim 39 (new): The ISA selection logic of claim 1, wherein boundary addresses are written to the plurality of boundary address registers during initialization of the CPU.

Claim 40 (new): The ISA selection logic of claim 1, wherein boundary addresses are altered by an operating system as application programs are fetched and loaded into memory.

Claim 41 (new): The ISA selection logic of claim 1, wherein software within a linker/loader program determines the boundary addresses that are loaded into the plurality of boundary address registers.

Claim 42 (new): The ISA selection logic of claim 1, wherein the ISA mode controller sequentially compares the address to boundary addresses stored in the plurality of boundary address registers.

Claim 43 (new): The processor of claim 20, wherein the plurality of boundary address registers store boundary addresses that represent lower address bounds for the plurality of address ranges.

Claim 44 (new): The processor of claim 20, wherein the plurality of boundary address registers store boundary addresses that represent upper address bounds for the plurality of address ranges.

Claim 45 (new): The processor of claim 20, wherein the plurality of boundary address registers store boundary addresses that partition the address space into a plurality of unequal address ranges.

Claim 46 (new): The processor of claim 20, wherein boundary addresses are written to the plurality of boundary address registers during initialization of the processor.

Claim 47 (new): The processor of claim 20, wherein boundary addresses are altered by an operating system as application programs are fetched and loaded into memory.

Claim 48 (new): The processor of claim 20, wherein software within a linker/loader program determines the boundary addresses that are loaded into the plurality of boundary address registers.

Claim 49 (new): The processor of claim 20, wherein the ISA mode controller sequentially compares the address to boundary addresses stored in the plurality of boundary address registers.

Claim 50 (new): A computer readable medium comprising a processor core embodied in software, the processor core comprising:

a plurality of boundary address registers for storing boundary addresses that partition an address space into a plurality of address ranges, each of the plurality of address ranges corresponding to one of a plurality of ISA decoding modes; and

an ISA mode controller that includes address evaluation logic,

wherein the ISA mode controller

receives an address of a program instruction to be decoded,

compares the address to boundary addresses stored in the plurality of boundary address registers, and

determines an ISA decoding mode for the program instruction based upon the comparison of the address to the boundary addresses.

Claim 51 (new): The computer readable medium of claim 50, wherein the plurality of boundary address registers store boundary addresses that represent lower address bounds for the plurality of address ranges.

Claim 52 (new): The computer readable medium of claim 50, wherein the plurality of boundary address registers store boundary addresses that represent upper address bounds for the plurality of address ranges.

Claim 53 (new): The computer readable medium of claim 50, wherein the plurality of boundary address registers store boundary addresses that partition the address space into a plurality of unequal address ranges.

Claim 54 (new): The computer readable medium of claim 50, wherein boundary addresses are written to the plurality of boundary address registers during initialization of the processor core.

Claim 55 (new): The computer readable medium of claim 50, wherein boundary addresses are altered by an operating system as application programs are fetched and loaded into memory.

Claim 56 (new): The computer readable medium of claim 50, wherein software within a linker/loader program determines the boundary addresses that are loaded into the plurality of boundary address registers.

Claim 57 (new): The computer readable medium of claim 50, wherein the ISA mode controller sequentially compares the address to boundary addresses stored in the plurality of boundary address registers.

Claim 58 (new): A method for determining ISA decoding modes for program instructions of a multiple-ISA application program running on a processor, wherein the application program includes instructions associated with a first ISA mode requiring a first amount of memory space and instructions associated with a second ISA mode requiring a second amount of memory space, and wherein the processor includes a plurality of boundary address registers and an ISA mode controller coupled to the plurality of boundary address registers, the method comprising:

(1) storing application program instructions associated with the first ISA mode in memory beginning at a first memory address;

(2) writing the first memory address to a first boundary address register of the plurality of boundary address registers, wherein the first memory address acts as a first boundary address that partitions the memory and creates a first memory address range;

(3) storing application program instructions associated with the second ISA mode in memory beginning at a second memory address;

(4) writing the second memory address to a second boundary address register of the plurality of boundary address registers, wherein the second memory address acts as a second boundary address that partitions the memory and creates a second memory address range;

(5) retrieving a program instruction form a third memory address;

(6) comparing the third memory address with the first memory address in the first boundary address register and the second memory address in the second boundary address register to determine whether the third memory address corresponds to the first memory address range or the second memory address range;

(7) generating, if the third memory address corresponds to the first memory address range, a first ISA mode indicator output with the ISA mode controller; and

(8) generating, if the third memory address corresponds to the second memory address range, a second ISA mode indicator output with the ISA mode controller.

Claim 59 (new): The method of claim 58, wherein a memory address having a value greater than the first boundary address and less than the second boundary address corresponds to the first memory address range.

Claim 60 (new): The method of claim 58, wherein a memory address having a value less than the first boundary address and greater than the second boundary address corresponds to the first memory address range.

Claim 61 (new): The method of claim 58, wherein step (2) and step (4) occur only during initialization of the processor.

Claim 62 (new): The method of claim 58, wherein step (2) and step (4) are performed by an operating system as application programs are fetched and loaded into memory.

Claim 63 (new): The method of claim 58, wherein step (6) comprises:

sequentially comparing the third memory address with the first memory address and the second memory address.

Claim 64 (new): A computer program product, embodied in a computer usable medium, for causing a multiple-ISA processor to partition a memory address space into memory address ranges associated with particular ISA modes, wherein the processor includes a plurality of boundary address registers and an ISA mode controller coupled to the plurality of boundary address registers, the computer program product comprising:

a procedure that causes the processor to store application program instructions associated with a first ISA mode in memory beginning at a first memory address;

a procedure that causes the processor to write the first memory address to a first boundary address register of the plurality of boundary address registers, wherein the first memory address acts as a first boundary address that partitions the memory and creates a first memory address range;

a procedure that causes the processor to store application program instructions associated with a second ISA mode in memory beginning at a second memory address; and

a procedure that causes the processor to write the second memory address to a second boundary address register of the plurality of boundary address registers, wherein the second memory address acts as a second boundary address that partitions the memory and creates a second memory address range.

Claim 65 (new): The computer program product of claim 64, wherein a memory address having a value greater than the first boundary address and less than the second boundary address corresponds to the first memory address range.

Claim 66 (new): The computer program product of claim 64, wherein a memory address having a value less than the first boundary address and greater than the second boundary address corresponds to the first memory address range.

Claim 67 (new): The computer program product of claim 64, wherein the memory space corresponding to the first memory address range is greater than the memory space corresponding to the second memory address range.